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Features of Electrophysical Diagnostics of Schottky Field Transistors Based on GaAs Epitaxial Layers on Silicon Substrates for Microsystem Applications

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In this paper, the structure of GaAs FET on a silicon substrate, suitable for local integration in the local SOI-technology and the method of its electrophysical diagnostics based on changes in the thermal resistance (R_T), are analyzed. It is known [3,4] that the thermal conductivity of GaAs is 3-4 times worse than silicon. To eliminate this disadvantage, the technology of forming high-speed GaAs-structures on the surface of the silicon substrate was proposed.

Keywords: gallium arsenide, FET, thermal resistance, electrophysical diagnosis.

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Introduction

The perspective elements for the creation of the element base of the microsystems-on-chip (MSoC) are silicon-on-insulator structures (SOI) which, due to the dielectric insulation of the device layer, have significant advantages over standard CMOS structures on bulk silicon with respect to speed, power consumption, element integration, etc. In addition, the SOI-structures open up additional possibilities for the new device structures creation, in particular, the sensory type, which is important for the creation of sensory and analytical MSoC [1,8]. According to the technologies of local SOI-structures, on one silicon chip, it is possible to integrate both device SOI-structures and arsenide-gallium transistors (GaAs), in particular, Schottky field effect transistors (Shottky FET). Such integration opens up wide opportunities for creating an elemental base of sensory MSoC.

It is known that the thermal conductivity of GaAs is 3-4 times worse than silicon. The possibility of using the value of R_T as an informative electrophysical parameter for the diagnosis of the device structures of integrated circuits (ICs) is based on the established sharp dependence of their reliability on temperature, namely, an increase in the temperature of the device at 15 ºC, the period of its operation decreases 2-6 times. The purpose of investigating the value of R_T integral GaAs epitaxial device structures on silicon substrates is to increase the lifetime of their operation to the level of silicon IC.

I. Features of forming gallium arsenide Shottky-FET on a heterojunction

A perspective element of high-speed ICs and MSoC (in the microwave range) created is a heterostructure field transistor with a conducting metal-semiconductor transition (GMeS), which uses the properties of the heterojunction between thin monocrystalline layers of two semiconductor materials with a close crystalline structure (crystalline lattice parameters), but with excellent widths of prohibited zones. The most common is the hetero p-n-transition between GaAs and arsenide-gallium-aluminum($Al_xGa_{1-x}As$), as shown in Fig. 1, a. The value of x indicates the relative content of aluminum. The width of the band gap Alx Ga1-xAs linearly increases with x. the typical value x = 0.3 which corresponds to the bandgap band Ep2 = 1.82 eV.

An equilibrium energy diagram of such a heterojunction between weakly alloyed GaAs and doped donor (Si, Se, S) Al_xGa_{1-x} As is given in Fig. 1, b. The horizontal line in the diagram corresponds to the Fermi level E_F. In equilibrium, this energy is the same for both types of semiconductors. In an unmanaged or weakly-fused semiconductor GaAs (area 3, the Fermi level is located almost in the middle of the bandgap), as in its own semiconductor i-type.

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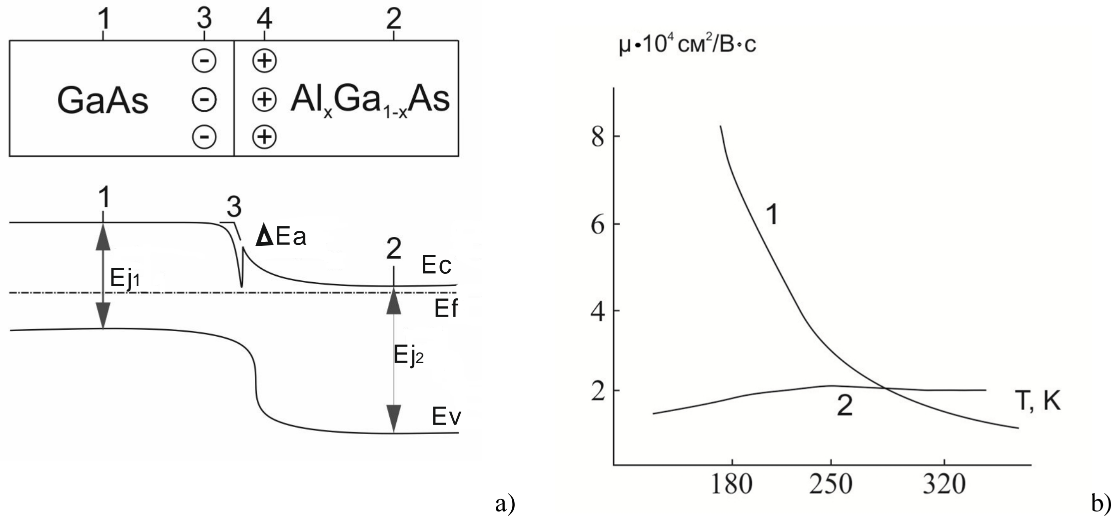

Fig. 1. Structure and equilibrium energy band diagram of the hetero p-n-junction between weakly alloyed GaAs and doped donor Si, Se, S) Al_xGa_{1-x} As (a), temperature dependence of electron mobility for a two-dimensional electron gas (2DEG) in the Al_xGa_{1-x} heterostructure -$_x$As (curve 1) and GaAs (curve 2) (b).

both types of semiconductors. In an unmanaged or weakly light semiconductor GaAs (area 3 Fermi level is placed almost in the middle of the bandgap). Its also called his own semiconductor (i-type). In doped donor semiconductor (region 2) Al_x $Ga_{1-x}As$ with concentration N_D = (1-20) $10^{17}cm^{-3}$, the Fermi level is placed near the bottom of the conduction band Ec. And in GaAs, at the boundary 5 of both semiconductors in the conduction band Ec, an area 3 with a minimum electron energy is formed. In this region, the accumulation of electrons from the region 4, located in $Al_xGa_{1-x}As$ (region 2), takes place through the created barrier. Region 4 is depleted of electrons and is charged positively, because it gives uncompensated donor ions. Here, the rupture of the bottom of the conduction band E_c (holds the jump ΔE_p) at the boundary of 5 with x = 0.3 by the value of 0.32 eV.

The electrons accumulated in the region 3 are located in a potential well and in a weak electric field can move only along the boundary 5 in the perpendicular plane in accordance with this figure. Therefore, such an aggregate of electrons accumulated in region 3 is called (2DEG), emphasizing that in the weak electric field these electrons can not move in the third dimension, that is, to move from region 3 to region 4, because there is a barrier formed the separation of the bottom of the conduction band and the jump of ΔEc.

Thus, 2DEG occurs due to the thermal ionization of donor impurities in the GaAs-Al region, where the concentration of donor impurities is $N_d > 10^{17}$ cm^{-3} and, with increasing mobility, they move to region 3 located in GaAs, where the concentration of donors is less than 10^{14} cm^{-3}.

Therefore, in such p-n-junction, the spatial separation of free electrons (in region 3) and the scattering centers (acceptor ions), concentrated in $Al_xGa_{1-x}As$, is achieved. This is the difference between the heterojunction of homotransitions. Due to the discrepancy of the crystalline lattice of two materials GaAs and $Al_xGa_{1-x}As$ on one side and GaAs and the silicon substrate through the buffer layer of germanium on the other side, a low surface density Q_{ss} and defects are provided because the silicon substrate already has a formed oxygen getter.

For the reasons given, for electrodes accumulated in region 3, a very high electron mobility μ=(8-9)10^3 cm^2/B s at a temperature of 300 ^{0}K is achieved in a weak electric field. Since the lattice scattering of carriers prevails in the unpolated epitaxial layer and GaAs, the mobility of electrons sharply increases with decreasing temperature to cryogenic (77 ^{0}K). For a better spatial separation of 2DEG and scattering centers between non-converted and-GaAs and doped with donor n-$Al_xGa_{1-x}As$, a thin (a thickness of several nanometers 4-6 nm) a buffer separating layer of the unaligned (i-$Al_xGa_{1-x}As$), which increases the mobility of 2DEG electrons, is introduced. The temperature dependence of the mobility of electrons for 2DEG in a heterostructure with a buffer layer is given in Fig. 1,b (curve 1).

At the temperature of liquid nitrogen (77 ^{0}K) and liquid helium (4 ^{0}K), the electron mobility increases from $1.4x10^5$ to $2x10^6$ cm^2/Vs, respectively. In the same figure, the temperature dependence of the electrons mobility in the layer and-GaAs (curve 2) containing donors with a concentration of $10^{17}cm^{-3}$ is given. This indicates that the speed of the SFET at the heterojunction is at least equal to that of the homotransition. The mobility of electrons of 2DEG, especially at cryogenic temperatures, strongly depends on the technology of formation of the heterostructure. Different methods of epitaxial buildup of thin epitaxial layers of GaAs on a silicon substrate are used for its formation: gas-phase, molecular-beam and atomic-layer epitaxy of organometallic compounds (OMC).

The best quality of the epitaxial layers in the given heterostructure, the smallest defect density at their limits and the greatest mobility is provided by the developed atomic-layer epitaxy using the photolysis of the expansion of the OMC using the KrF excimer laser. GaAs low thermal conductivity and resulted in the development of arsenide-gallium technology on the

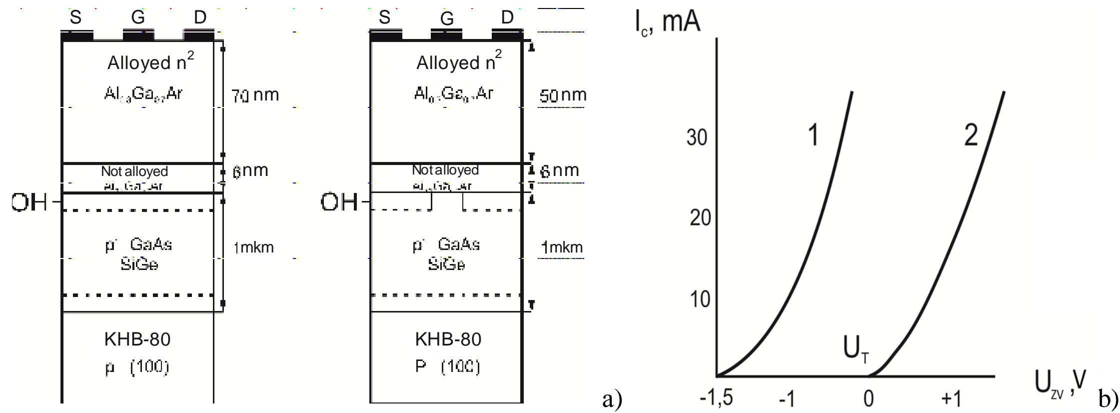

Fig. 2. Structure of normally open (1) and normally closed (2) SFT-transistors on the heterojunction a): their drain-gate characteristics b).

epitaxial layers deposited on silicon substrates with high thermal conductivity, which greatly improves thermopole stability of the parameters of sub-micron structures of VLSI and SoC, which is diagnosed by the value of the thermal resistance R_T.

The above heterogeneous transitions can be used for high-speed VLSI and SoC based on SFT (metal-semiconductor transition). Examples of SFT-structures with normally open and closed GeMeS (SFT - transistors are shown in Fig. 2, a, and their transmission characteristics in Fig. 2, b.

In the formation of structures of normally open PTSL on the silicon substrate by atomic-layer epitaxy using OMC and activation with the KrF excimer laser at $T \approx 520^0C$, a buffer layer of germanium is applied to equalize the constant silicon lattices and gallium arsenide and the layers of weakly polished p-GaAs region and non-alloyed and n+-layer $Al_xGa_{1-x}As$.

The latter is doped with selenium to the value N_d = (5-7) 10^{17} cm^{-3}. For the formation of the gate 3, a film of aluminum alloy AlSiGo11 (aluminum-silicon-holmium) is used, and for the lead contacts of the lead areas, the alloy AuGe12 (AuGeNi). In a normally closed transistor, the upper layer of arsenide-aluminum-aluminum is partially applied to a thickness of 50 nm. In this way, on a single silicon substrate, both normally open and normally closed SFT are formed, which form a complementary CSFT.

Threshold voltage of such SFT transistors is determined by the formula:

$$U_T = \varphi_{03} + \frac{\Delta E_{\Pi}}{q} - qN\Delta \cdot d^2/2\mathcal{E}_0\mathcal{E}_{n2}, \quad (1)$$

where φ_{03} is the equilibrium height of the potential transition barrier metal-semiconductor (GaAsAl); where the total thickness of donor doped and non-doped GaAsAl layer; ε_{n2} its relative dielectric constant.

The principle of the GMeS transistor is similar to the principle of the transistor interconnect on homo transmissions, as SFT. Between the metal gate and the GaAsAl layer placed below it, a so-called controlling heterojunction (metal-semiconductor) is formed. The depleted region of such a transition is mainly located in a GaAsAl layer. The channel of a normally open transistor is formed at Ugs <0 in the non doped GaAs-layer at the boundary with the OH 2DEG heterojunction, which is limited by the dashed line in Fig. 2, a.

Under the influence of the control voltage, the gate-source changes the thickness of the depleted region of p-n - the transition (barrier) of the metal-semiconductor, the electrons concentration in the OH and the drain current. The electrons enter the OH from the source. With a sufficiently large (by the module Ugs <0), which is equal to the threshold voltage U_T, the depleted transition region expands to the extent that it completely overlaps the OH electrons and the drain current becomes zero.

In a normally closed SFT, due to the smaller thickness of the GaAsAl upper layer at Ugs = 0, the conducting channel is absent, since the region of accumulation of 2DEG is completely blocked by the depleted region of the control p-n-junction. And the channel opens even with some positive voltage Ugs> 0, if the impoverished domain of the control transition is narrowed to such an extent that its lower boundary falls into the region of electron accumulation. Based on Fig. 2,b, we obtain a complementary pair of transistors on a heterojunction.

In Fig.2,b, the drain-gate characteristics of such a complementary pair of SFTs are presented, that is, normally open 1 and normally turned off 2 transistors with a gate length L= 0.5μm at a drain flow distance of 2.5μm with the thickness of the layers given in Fig. 2, a. Due to the high mobility of OH (2EDG) at a small gate length almost in the whole range at the gate voltage U_{gs} (except for U_T) saturation of electrons drift velocity is reached over 10^7 V/s and the linear dependence of the drain current I_d is observed:

$$I_c = s'(U_{3\text{B}} - U_{\text{T}} - E_{\text{KP}} \cdot L_{\text{K}}), \quad (2)$$

where E_{CR} - critical field strength; $S' = S/(1 + R_{\text{B}} \times S)$; $S = \epsilon_0 \epsilon_{0\Pi} V_{n\,kr} \times b/d$.

For curves 1 and 2, S '/b is equal to 117 and 175 mS/mm, respectively. The high value of the slope of a normally closed SFT (curve 2) is due to a lower thickness doped by donors n+ - $Al_xGa_{1-x}As$. And the high value of steepness significantly increases the speed accordingly.

A very important advantage of the structure of GMeS-transistors (SFT) on the heterojunction is the lower surface-charge Q_{ss} density on the GaAsAl

boundary with the dielectric (SiO_2, Si_3N_4) and the Schottky barrier height is φ_{0g} = 1V in comparison with the transistors of the MeS on the homogeneous transition. Therefore, due to the lower density of the surface charge Q_{ss}, the negative superficial charge and the thickness of the impoverished regions in the drainage, shutter-drain, and thus less parasitic resistance of these regions are reduced without the use of additional technological operations of selective ion-type doping (LDD) which required for transistors with self-aligned gates.

Due to the increased height of the Schottky barrier for the GMeS (SFT-s), a high (up to 0.7V) direct voltage-gate-source is permissible, which is especially important for normally closed SFTs, if the working voltages on the gate can vary in a rather narrow range, limited to the voltage at the control of the metal-semiconductor transition control.

The impulse and frequency properties of GMeS-transistors are mainly determined by the time of the passage of electrons through the channel, where they move with the saturation velocity: $t_{prk} = L_z / V_{sat}$. At T = 300 ^{0}K, and Vsat = $2 \cdot 10^7$cm/s, the temperature decreases with increasing the saturation rate by the law of Vsat~ 1/T. It is GSFT-transistors that are very replaceable for use in microwave VLSI and SoC. The best parameters of these transistors are at cryogenic temperatures (77 ^{0}K). However, at room temperature, their main parameters (noise and gain) are better than in the SFT - transistors on the homotransition, which is achieved and with a greater length of the gate GMeS - transistors. For example, in the frequency range 18-30 GHz, the MeS transistors with a gate length L = 0.25 μm have a noise ratio of 1.8 dB and a gain of 9 dB. Similar values of these parameters for GMeS-transistors are obtained with a gate length Lg = 0.4 μm. At present time, GMe transistors on GaAs on silicon substrates are already being developed with a gate length of 0.18 - 0.2 μm, which can operate at microwave frequencies up to 125 GHz.

So, as can be seen from the research results - to predict the reliability of such high-speed LSI, formed on the basis of epitaxial GaAs GMeS-transistors, it is necessary to choose the method of electrophysical diagnostics, starting with of the structures formation stage. The so-called thermal resistance R_T was chosen for this because it determines the quality of the buffer germanium layer Si-Ge between the silicon substrate formation and the epitaxial layer of GaAs to equalize the permanent crystalline lattices, which arise both through epitaxy and multiply charged germanium implantation (Ge ++). Therefore, consider the features of this method.

II. Electrophysical diagnostics of GGST - transistors of high-speed LSI on epitaxial layers of GaAs formed on Si-substrates.

The physical nature of the thermal resistance R_T is that, when scattering in the process of operation of a semiconductor device, as part of the LSI part of the electric power supplied to it, it is converted into heat coming from the corresponding heat path to the thermal drain which is in the semiconductor device or integral element of the environment, and at considerable power - a special heat dissipation - a radiator was created.

When a non-stationary transitional thermal process in the LSI, it is necessary to take into account the value of the heat capacity and then the heat path will represent the R_TC_T gain [2,4]. Transient and parallel thermal resistances have their own diagnostic information, which is difficult to evaluate in the transient space. The thermal conductivity of the LSI structure on the Si substrate, the housing, the radiator or the tape carrier (the frame is deduced), because the LSI structure itself is heterogeneous.

Of all the known methods for the temperature measuring of the LSI crystal and the evaluation of the R_T thermal resistance on this basis, the electrophysical method (or the method of the thermosensitive parameter) prevails due to its advantages: the simplicity of the circuit implementation, the ability to measure the temperature of the test element of the LSI without direct access to her, the ability to measure the most overheated areas of the structure. It is precisely for GaAs field transistors with the form gate as a Schottky barrier such thermosensitive elements that can be: source resistance,

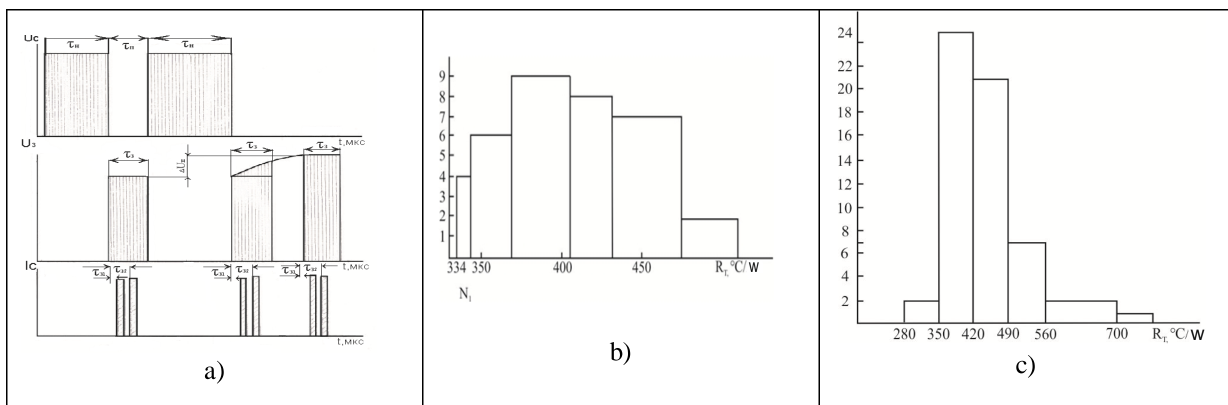

Fig. 3. Meter of thermal resistance R_T for field and bipolar transistors and its structures for the electrophysical diagnosis of their reliability a) and the diagram of the meter work of thermal resistance for the PTM b, c).

resistivity of the gate system with metallization, direct voltage drop in the gate-source gain ΔU_{gs}, which were chosen in this paper for the electrophysical diagnosing SFT on Si-substrate.

In general, the thermal resistance is determined from the following relationships:

$$U_{\text{ЗВ}} = \varphi_0 - K_{\text{T}}\left(T_{\text{C}} + R_{\text{T}} \times P_{\text{розс}}\right), \quad (3)$$

Where φ_0 is the magnitude of the potential Schottky barrier (V); K_T - coefficient of thermosensitivity; P_{sc} is the power of scattering.

By differentiating the expression (3) in turn in terms of P_{ps} and the temperature of the medium of the T_C, taking the ratio of these derivatives in the finite difference, we obtain the thermal value of resistance:

$$R_T = \frac{[[\Delta U_{\text{ЗВ}}(P)/\Delta P_{\text{розс}}]_{T_c}]}{[\Delta U_{\text{ЗВ}}(T)/T]_{\text{розс}}} \quad (4)$$

Here, the values of ΔU_{gs} (P) and ΔU_{gs} (T) represent a change in the thermosensitive parameter caused by the change of only the external power scattering or only the external temperature, respectively.

From the obtained relation (4) it is evident that in order to determine the thermal resistance R_T it is necessary to measure the pit (per) unit of dissipation power of the heat-sensitive growth parameter under thermostatting conditions (T_S = const) and divide it into increment of this parameter already obtained at change of external temperature, when P_{SC} = const = 0, that is, on the temperature coefficient of the thermosensitive parameter $K_{T.}$

This method was developed and tested in the electrophysical diagnostics laboratory of bipolar and field transistors structures in SCTB "Orizon" (JSC "Rodon"). The R_T thermal resistance meter for typical bipolar and field transistors (Fig. 3) in the automated test electrophysical diagnostics of the LSI reliability includes: a thermosensitive parameter meter, a thermostat and a control unit with a contacting device for sealed transistors and integrated test structures. Diagram of R_T meter operation is shown in Fig. 3 a, b, c.

The meter provides a calibration-calibration mode (on the special test transistor structures), at which from the control unit signals are received that provide the regulation and thermostaturing of the contacting device at a given temperature range (-60 - +150^{0}C) ± 1^{0}C. The value of the temperature thermal sensitivity parameter Kт (B/^{0}C) is defined as the average of the total number of measurements (5-10)[5,7].

In the R_T measurement mode, the oscillating generator generates a pulse of U_{DS} with a certain duration τ_i and a pause τ_p, which determines the heating time and the duration of the heating power pause, as well as the measurement voltage and stroke pulse value. The pulse of the heating power through the amplifier enters the electric circle of the flow of the investigated SFT, and the pulses of the measuring voltage through the amplifier and the current-setting element in the electric range of the measured test transducer GeSFT at the moment of the heating power pause, as shown in the diagram of Fig. 3, b.

The voltage at the gate U_{gs} and its gain ΔU_n is measured by a pulse amplitude voltmeter. Both the gate current and voltage (as a gate pulse, including a pulse voltmeter) are measured here at two set time intervals τ_r = 0.5 µs and τ_{r2} = 1.5 µs. The original use of the double gating pulse in the R_T thermal equalizer in GaAs- GeSFT is due to the following factor. It is GaAs- GeSFT transistors on the Si-substrate of the microwave band due to the participation of 2DEG, as a rule, designed to operate in the high frequency region (> 5 GHz) and therefore have a rather thin nanometer active structure. In addition, the estimation of the power dissipation even in the ideal SFT structure shows the possibility of unequal distribution of currents (and hence heat) that heat such a multilayer structure along the channel width and its length, and the presence of a buffer layer (Ge-Si) and defects of the constant lattice coefficients in the topology only exacerbate this uneven heating.

Taking into account the lower thermal conductivity of GaAs in comparison with mono-Si, it results in a much sharper expression of the localized heating of the buffer layer in the GaAs-GeSFT-structure. Therefore, the GaAs-GeSFT - structure should be considered as a parallel coupled heat capacity and thermal resistance R_T. The work cycle defined by the diagram Δ, including the pulse period τ_1, when the electrical power P is applied to the structure; and the period τ_2 during which the structure cools. Such heating and cooling cycle can be described by the equation:

$$P = C\frac{dT}{dt} + \frac{T}{R_T}\ ,\ T = \begin{cases} T_0 & \text{при } t = \mathbf{0} \\ T_1 & \text{при } t = \tau \end{cases} \quad (5)$$

The expanding uniformity is described by:

$$T = PR_T(T_0 - PR_T)\mathbf{exp}(-{}^{t}/_{\tau}) \quad (5')$$

where $t = R_T C$ is the thermal characteristic of the technological epitaxial layer;

And the process of the GeSFT- structure cooling can be described in a similar way:

$$O = C\frac{dT}{dt} + \frac{T}{R_T}\ ,T = \begin{cases} T_0 & \text{при } t = \mathbf{0} \\ T & \text{при } t = \tau_2 \end{cases} \quad (5'')$$

However, this cooling process changes the temperature by the expression:

$$\text{T} = T_1\mathbf{exp}(-{}^{t}/_{\tau}), \quad (5''')$$

where, T_0, T_1, T_2 are the initial temperatures for each process.

Then, in thus established cyclic process, the maximum and minimum temperatures are set over a certain period of time, that is, a certain difference thereof, which ensures equality during the period of cooling with heat and heat, which is fed to the GaAs-GeSFT -structure during the heating period. From the power balance equation we obtain these values of maximum and minimum temperature, which are expressed as:

$$T_{max} = PR_r\frac{\mathbf{1} - exp\left({}^{-\tau_2}/_{\tau}\right)}{\mathbf{1} - exp\left({}^{\Delta}/_{\tau}\right)},$$

$$T_{min} = PR_r\frac{exp\left({}^{-\tau_1}/_{\tau}\right) - exp\left({}^{-\Delta}/_{\tau}\right)}{1 - exp\left({}^{-\Delta}/_{\tau}\right)}, \quad (6)$$

where, PRr is the maximum possible temperature in a given heterogeneous system at $\tau_1 \to \infty$. This calculation is made for a continuous sequence of heating pulses. The largest temperature drop is created by the buffer Ge-Si layer. To minimize this transition, the formation of this layer was investigated by both the epitaxy process and the multi-charge ion implantation of germanium (Ge^{++}). This temperature difference may be different for normally open and normally closed GaAs-GeSFT.

Therefore, we see that the heat output from the test

transistor structure after the end of the heating pulse sequence along the thermal path is most fully described by a set of exponents of the transient thermal process with the corresponding thermal constants t_i.

To analyze the mode of measurement of R_T in GaAs-GeSFT in the first approximation can be taken a single exponent of $\tau_i = \tau_{min}$. Analytical estimation of such process, which is carried out above in the process of heating-cooling, gives a value, that is, when the value $\tau_i \approx \mathbf{5}$ мкс of the first tuned sling pulse from the back edge of the heating pulse t_{31} = 0.5mks, the change in temperature in the buffer layer can be 25-30% for the ideal structure (defect-free) , and in the real 35-40%.

The originality of this method is the introduction of a second strobe pulse, which makes it possible to amend the temperature of the GaAs-GeSFT active zone and thus to estimate the true buffer layer temperature for the complementary pair of GeSFT at the moment of heating pulse activation:

$$T_0 = T_1 \exp\left(\frac{\tau_{31}}{\tau_{32}-\tau_{31}} ln\frac{T_1}{T_2}\right) = T_1 K_T, \qquad (7)$$

where T_1 and T_2 are the temperature of the GaAs-GeSFT- structure, measured from the delayed τ_{31} and τ_{32} of Fig. 3,b respectively.

Parameters of R_T thermal resistance meter, which performs electrophysical diagnosis of GaAs-GeSFT on the Si-substrate, are as follows:

1). The voltage range of the heating power at a current of 0.5 A - (0-20) ± 1V;

2). The range of positive and negative polarity bias voltage for a normally open and normally closed GeSFT – (0-10) V;

3). The range of measuring the increase of the thermosensitive parameter is (0-1000) ± 1% mV;

4). Thermostat range is (-60 + 150) ± 10 ^{0}C.

In Fig. 4 a, b the results of electrophysical diagnostics on the thermal resistance of the complementary structures of GaAs-GeSFT on Si-substrates, where the formation of the buffer layer was carried out by the epitaxial deposition of the germanium monolayer, are presented. As we see, the value of the time correlation K_T was in a rather good difference with the pre-calculated value of K_T = 1.26; as expected in real structures, the value of K_T takes values of 1.34 and 1.37.

Conclusions

1. Technologies of the formation of complementary GaAs-GeSFT on Si-substrates using the Ge-Si buffer layer between GaAs and Si-substrate are proposed.

2. The results of studies of the Ge-Si buffer layer are provided to ensure the alignment of permanent crystalline lattices between epitaxial GaAs and mono-silicon substrate using both the Ge-Si layer epitaxial deposition process and Ge ++ multiply charged ion implantation (Ge ++) in monosilicon.

3. A special test meter for thermal resistance for GeSFTs has been developed and an appropriate methodology has been developed that allows an electrophysical diagnostics of the quality formation of a buffer layer in complementary GaAs – GeSFT – structures on Si substrates.

4. Experimental research has shown that the diagnostics of the buffer layer on the parameters of thermal resistance R_T in the complementary structures of GaAs SFT on Si-substrates, can be implemented in the serial production of integral devices.

5. The developed methodology of test diagnostics of the SFT-structures for the thermal resistance parameters RT can be used also for the diagnosis of field transistors in the case design with the montage of an IC crystal in the package through the eutectic or on the tape carrier through the conductive adhesive or dispersed nickel gaskets.

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[1] S.P. Novosyadly`j, Sub- i nanomikronna texnologiya struktur VIS (: Misto NV, Ivano-Frankivs`k, 2010).
[2] S.P. Novosyadly`j, A.I. Terlecz`ky`j, Diagnosty`ka submikronny`x struktur VIS: monografiya (Simy`k, Ivano-Frankivs`k, 2016).
[3] D.Y`. Zaks, Параметры teplovogo rezhy`ma poluprovodny`kовых my`krosxem (Rady`o y` svyaz`, Moskva, 1983).
[4] C. Canali, F. Chiussi, G. Donzelli, E. Zanoni, Microelectronics Reliability 29(2), 117 (1986).
[5] A. L. Zaxarov, E. Y`. Asvadurova, Raschet teplовых parametrov poluprovodny`kовых pry`borov (Rady`o y` svyaz`, Moskva, 1989).
[6] S.P. Novosyadly`j, B.S. Dzundza, V.M. Gry`ga, M.V. Koty`k, S.V. Novosyadly`j, V.I. Mandzyuk, Sxidno-yevropejs`ky`j zhurnal peredovy`x texnologij 5/5/89, 26 (2017).
[7] Yu.M. Kalny`bolotsky`j, Yu.V. Korolev, G.Y`. Bogdan, B.C. Rogoza, Raschet y` konstruy`rovany`e my`krosxem (Vy`shha shkola, Ky`yiv, 1983).
[8] I.T. Kogut, V.I. Holota, A.A. Druzhinin, V.V. Dovhiy, Journal of Nanoresearch 39, 228 (2016). DOI: 10.4028/www.scientific.net/JNano R. 39.228.

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Особливості електрофізичного діагностування польових транзисторів Шотткі на епітаксійних шарах GaAs на кремнієвих підкладках для мікросистемних використань

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В даній статті проаналізовано структуру арсенід галієвого ПТШ на кремнієвій підкладці, придатного для локальної інтеграції в КНІ-технології та метод його електрофізичного діагностування на основі змін теплового опору R_T. Відомо, що теплопровідність GaAs в 3 - 4 рази є гіршою порівняно кремнієм. Щоб усунути цей недолік було розроблено технологію формування приладних швидкісних GaAs-структур на поверхні кремнієвої підкладки.

Ключові слова: арсенід галію, польовий транзистор, тепловий опір, електрофізичне діагностування.